AMENDMENTS TO THE CLAIMS:

Complete Listing of Claims

Claim **1** (canceled)

1   Claim **2.**   (currently amended) The system according to claim **8**, wherein the
2   serial link is chosen from one of the following: LVDS, Gigabit Ethernet,
3   InfiniBand, IEEE1394, RF Wireless, Infrared Wireless, or any combination of
4   these.

1   Claim **3.**   (currently amended) The system according to claim **8**, wherein the
2   host bus is a PCI bus.

1   Claim **4.**   (original) The system according to claim **2**, wherein the host bus is
2   an LPC (Low Pin Count) bus as defined by Intel 1997.

Claims **5 - 7** (canceled)

1   Claim **8**. (currently amended) <u>A system for extending a signal path of a host bus</u>

2   <u>comprising:</u>

3   <u>a first repeater portion connected to a first segment of the host bus;</u>

4   <u>a second repeater portion connected to a second, non-hierarchical</u>

5   <u>segment of the host bus remote from the first segment of the host bus, where</u>

6   <u>the first and second portions of the repeater are connected by a serial link,</u>

7   <u>wherein at least one of the repeater portions further comprises:</u>

8   <u>an interface to the first bus segment;</u>

9   <u>a transaction queue with a data buffer connected to the interface;</u>

10   <u>a link translation layer connected the transaction queue to translate</u>

11   <u>incoming transactions from the first bus segment into serial streams to be sent</u>

12   <u>over the serial link</u> ~~The system according to claim~~ **~~5~~**, further comprising a

13   transaction decode circuit connected to the interface to the <u>first</u> ~~host~~ bus

14   segment to determine which transactions on the <u>first</u> ~~host~~ bus <u>segment</u> to accept

15   and pass on over the serial link.

Claims **9** -**14** (canceled).